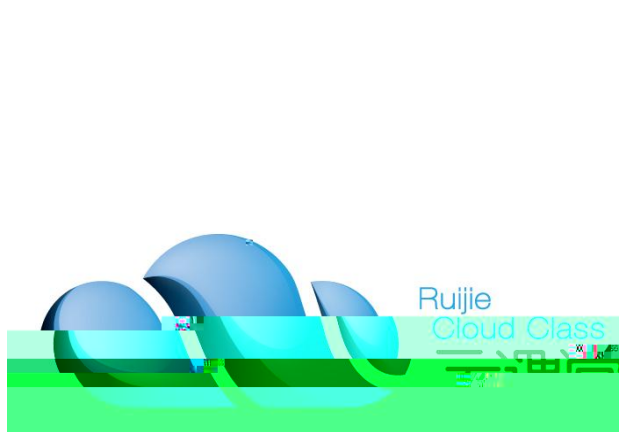




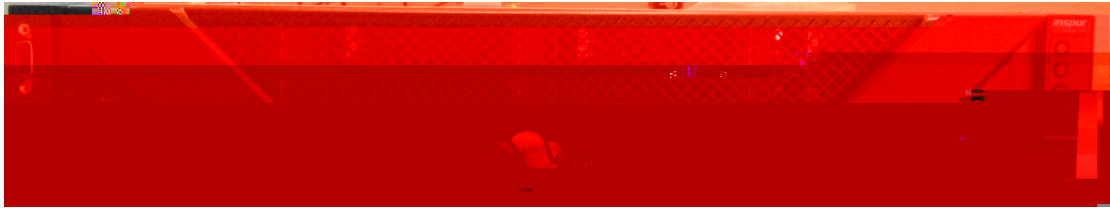
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2

2.1

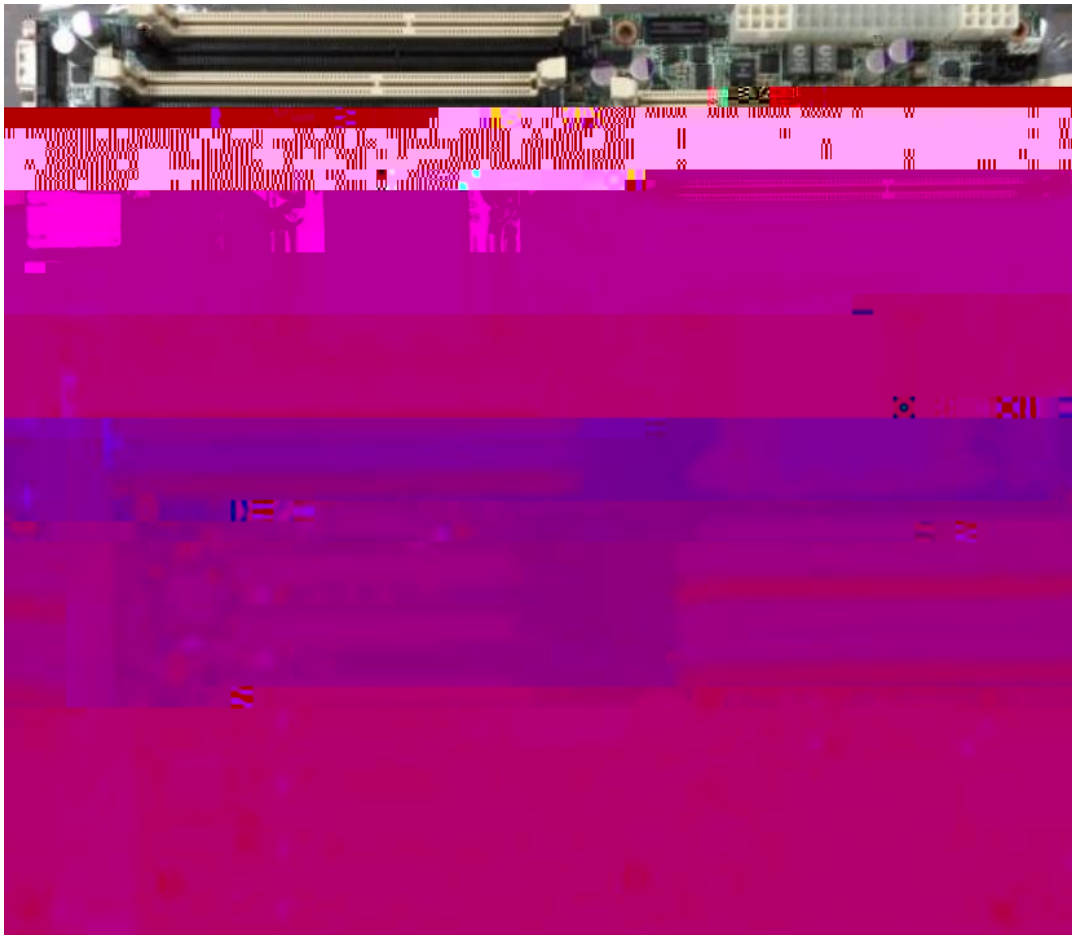
V1

V2



2.2 V1

2.2.1 V1

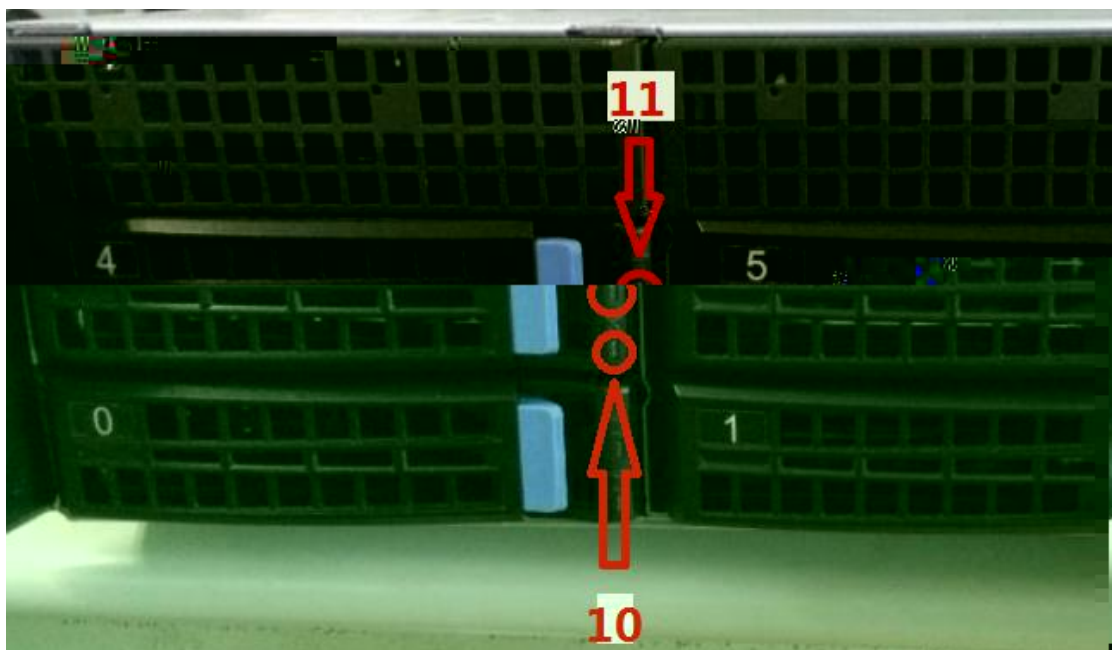
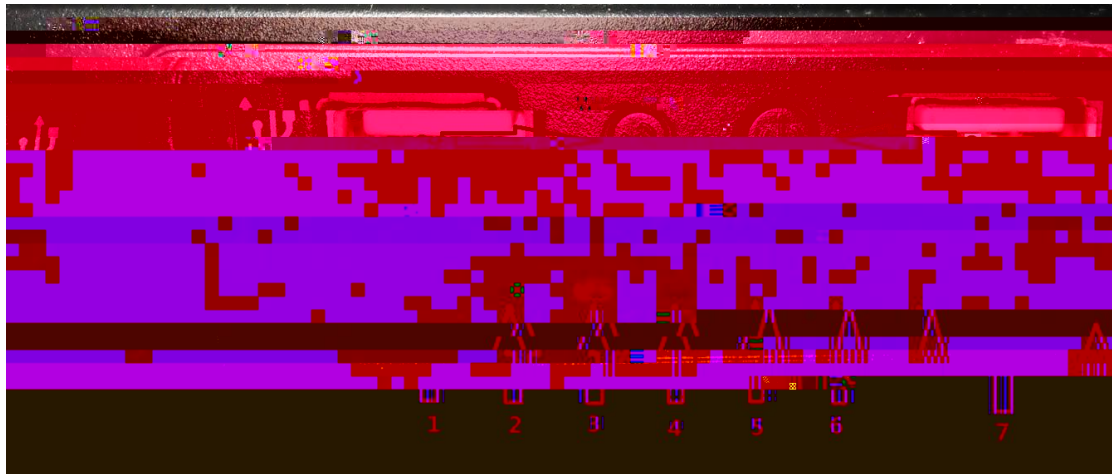


2.2.2 V1

2.2.3 CPU

2.2.4 CLR_CMOS

2.2.5



[illegible]

2.3 V2

2.3.1 V2

	()

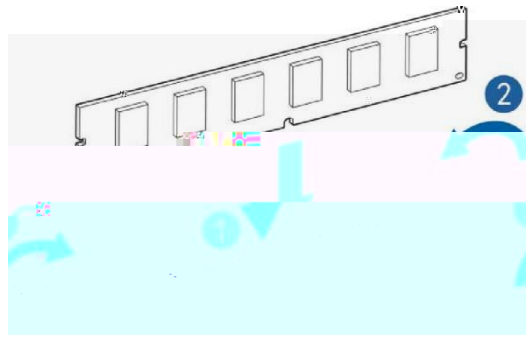
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V2



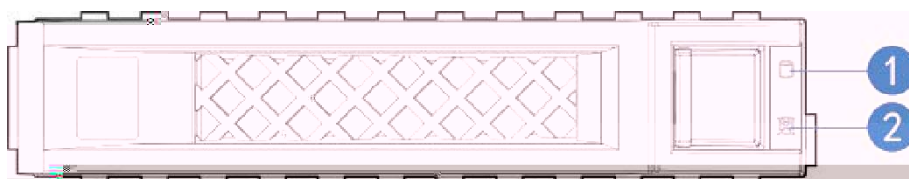
:
:
CHB_1/CHC_1/CHD_1/ CHA_2/ ” ”
CHD_0,CHA_1 ” ”

” ”

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2:
,
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2.3.3

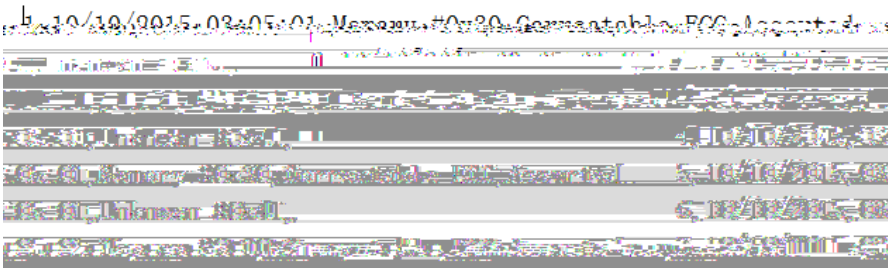


3.1.1

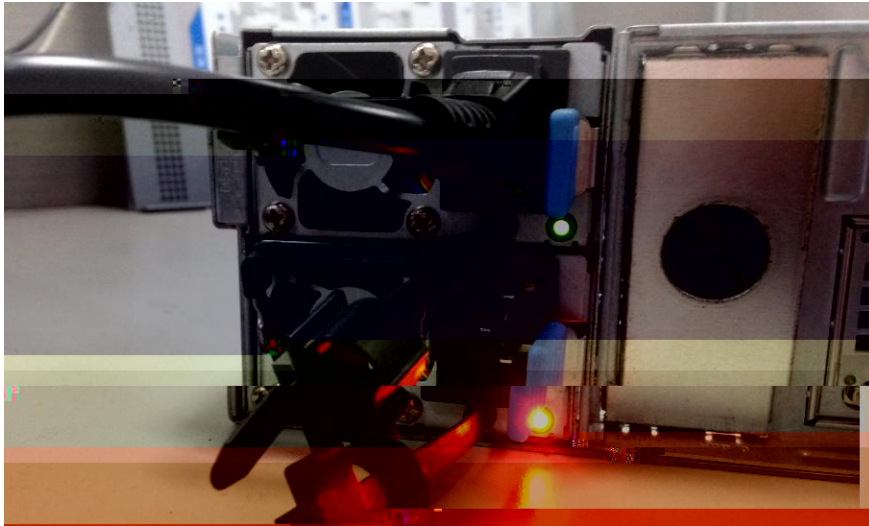
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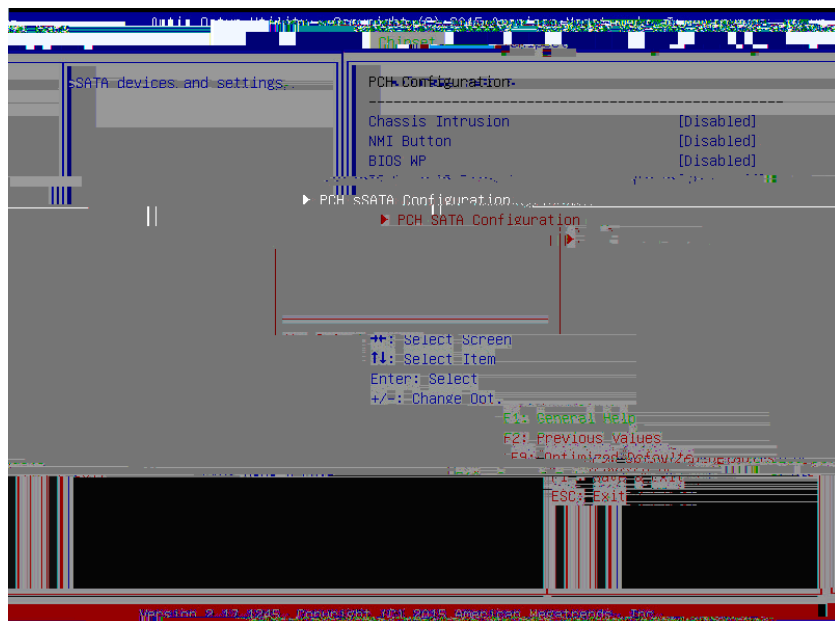
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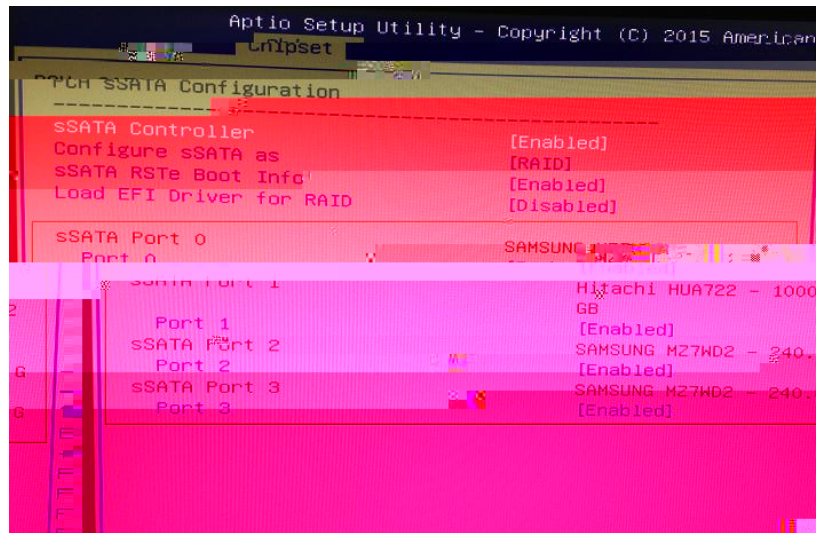


3.1.2



3.2.2





3.4.2

3.5

3.5.1

3.5.2

3.6

3.6.1

3.7.2

4

